WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first conductive film serving as a floating gate and formed on a semiconductor substrate via a first gate insulating film;

a second conductive film serving as a control gate and formed on the first conductive film via a second gate insulating film; and

a third conductive film buried in a contact hole formed by removing a part of the second conductive film and second gate insulating film so as to reach an upper surface of the first conductive film from an upper surface of the second conductive film.

2. The semiconductor device according to claim 1, wherein the third conductive film buried in the contact hole is formed of a conductive material different from that of the second conductive film serving as the control gate.

3. The semiconductor device according to claim 2, wherein the third conductive film is buried in the contact hole via a barrier metal.

4. The semiconductor device according to claim 1, wherein the third conductive film buried in the contact hole and the second conductive film serving as the control gate are formed of a silicon film, whose surface is converted into a silicide.

5. A semiconductor device comprising:

a nonvolatile semiconductor memory cell having a stacked gate formed by stacking a floating gate and a control gate above a semiconductor substrate; and

a transistor other than the memory cell, formed by stacking a first conductive film serving as the floating gate and a second conductive film serving as the control gate and bringing the first and second conductive films electrically into contact with each other, thereby forming gate wiring,

wherein, in the transistor portion other than the memory cell, a third conductive film is buried in a contact hole formed so as to reach an upper surface of the first conductive film from an upper surface of the second conductive film.

6. The semiconductor device according to claim 5, wherein the third conductive film buried in the contact hole is formed of a conductive material different from that of the second conductive film serving as the control gate.

7. The semiconductor device according to claim 6, wherein the third conductive film is buried in the contact hole via a barrier metal.

8. The semiconductor device according to claim 5, wherein the third conductive film buried in the contact hole and the second conductive film serving as the control gate are formed of a silicon film, whose surface is converted into a silicide.

9. The semiconductor device according to claim 5, wherein a nonvolatile memory cell array is formed by arranging a plurality of NAND cell units each being formed by connecting a plurality of said nonvolatile semiconductor memory cells in series, in a memory region; and

the third conductive film is buried in the contact hole of a selective transistor formed on at least one side of the serial nonvolatile semiconductor memory cells and in the contact hole of a peripheral transistor formed in a peripheral circuit region of the semiconductor substrate.

10. The semiconductor device according to claim 9, wherein the third conductive film buried in the contact hole is formed of a conductive material different from that of the second conductive film serving as the control gate.

11. The semiconductor device according to claim 10, wherein the third conductive film is buried in the contact hole via a barrier metal.

12. The semiconductor device according to claim 9, wherein the third conductive film buried in the contact hole and the second conductive film serving as the control gate are formed of a silicon film, whose surface is converted into a silicide.

13. The semiconductor device according to claim 9, wherein, in the selective transistor, the contact hole

is formed by removing part of the second conductive film and an insulating film formed between the first and second conductive films including one side of the gate wiring.

14. The semiconductor device according to claim 9, wherein, in the peripheral transistor, the contact hole is formed by removing the entire part of the second conductive film and an insulating film formed between the first and second conductive films.

15. A method of manufacturing a semiconductor device, comprising:

stacking a first gate insulating film, a first conductive film serving as a floating gate, a second gate insulating film, and a second conductive film serving as a control gate on a semiconductor substrate, thereby forming a gate wiring pattern of a stacked gate structure;

removing part of the second conductive film and the second gate insulating film, thereby forming a contact hole reaching an upper surface of the first conductive film from an upper surface of the second conductive film; and

burying a third conductive film in the contact hole.

16. The method according to claim 15, wherein the contact hole is formed after an insulating film for planarization is buried in a space in the gate wiring

pattern.

17. A method of manufacturing a semiconductor device, comprising:

forming a first conductive film serving as a floating gate on a semiconductor substrate via a first gate insulating film;

selectively etching the first conductive film serving as the floating gate so as to remove at least an unnecessary portion in a gate-width direction of the floating gate,

forming a second conductive film serving as a control gate on the substrate and on the first conductive film via a second gate insulating film;

selectively etching the second conductive film together with the first conductive film, thereby forming a gate wiring pattern for each of a nonvolatile semiconductor memory cell and a transistor other than the memory cell;

selectively etching the second conductive film and second gate insulating film by lithography in accordance with the gate wiring pattern in the transistor other than the memory cell, thereby forming a contact hole reaching an upper surface of the first conductive film from an upper surface of the second conductive film; and

burying a third conductive film in the contact hole.

18. The method according to claim 17, wherein the contact hole is formed after an insulating film for planarization is buried in a space in the gate wiring pattern.

19. The method according to claim 18, wherein, after the insulating film for planarization is buried in the space in the gate wiring pattern, a resist pattern is formed which has an opening in which part of the gate wiring pattern including one side thereof is exposed in a selective transistor region of the nonvolatile semiconductor memory cell, and then etching is performed for forming the contact hole with the resist pattern used as a mask.

20. The method according to claim 18, wherein, after the insulating film for planarization is buried in the space in the gate wiring pattern, a resist pattern is formed which has an opening in which the entire gate wiring pattern is exposed in a predetermined peripheral transistor region, and then etching is performed for forming the contact hole with the resist pattern used as a mask.